For Day 2

By All

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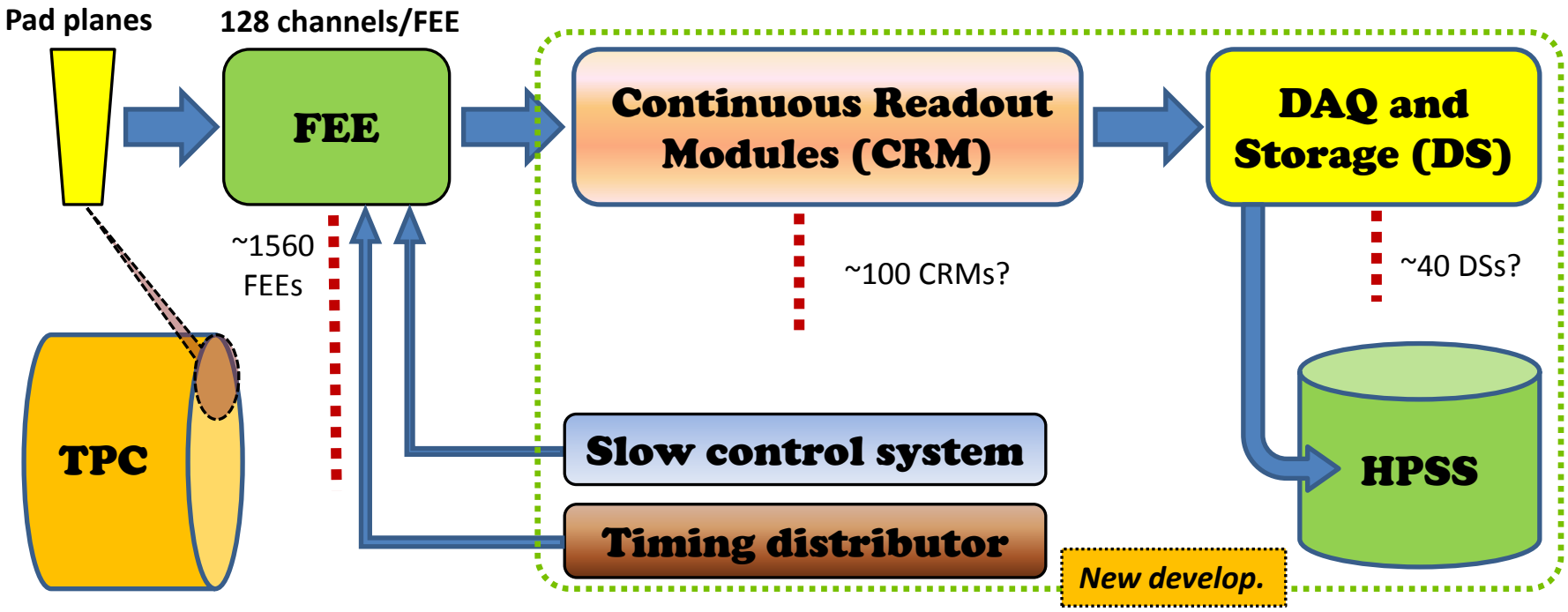
Numbers for baseline design

- 100K channels as the baseline
  - Half of full instrumentation, which is 200K
- 15KHz is the baseline trigger rate, since DAQ can't take data more than that.
  - Beam interaction may happen as much as 100KHz for |z|<1m
- dN_{ch}/dy = 180 (minbias Au+Au@200GeV) → 400 tracks in $|\eta|<1.1$
  - Accounting for fake tracks that double # of tracks, we assume 800 tracks
- 48 (radial) * 2 measurements/track, 8 bytes/measurement
  - Clustered data. Raw data will be higher.
  - 768 bytes/track. A factor of 2 comes from charge sharing between 2 pads
- ~0.6 MBytes/event → 60 GBytes/s (assuming 100 KHz in average)
  - Optical cable: 3.2Gbits/s = 0.4GBytes/s. → Need 150 fibers at minimum?
  - 5200 TB/day (100% running efficiency)
- An option of data volume reduction
  - 1/2 size data volume per track → 380 bytes/track, 0.3 MBytes/event, 30 GBytes/s, 2600 TB/day

sPHENIX TPC readout block diagram

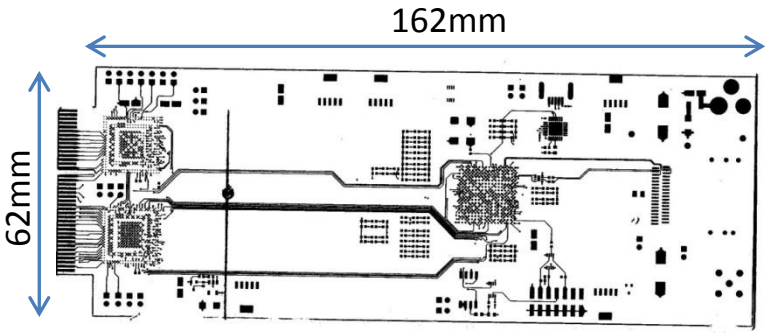
- 128 channels/FEE card: 4 SAMPA chips on one board
- 200K channels = 1563 cards. With 30% spares, 2032 cards
- Reading out data from FEE cards via Copper cable?

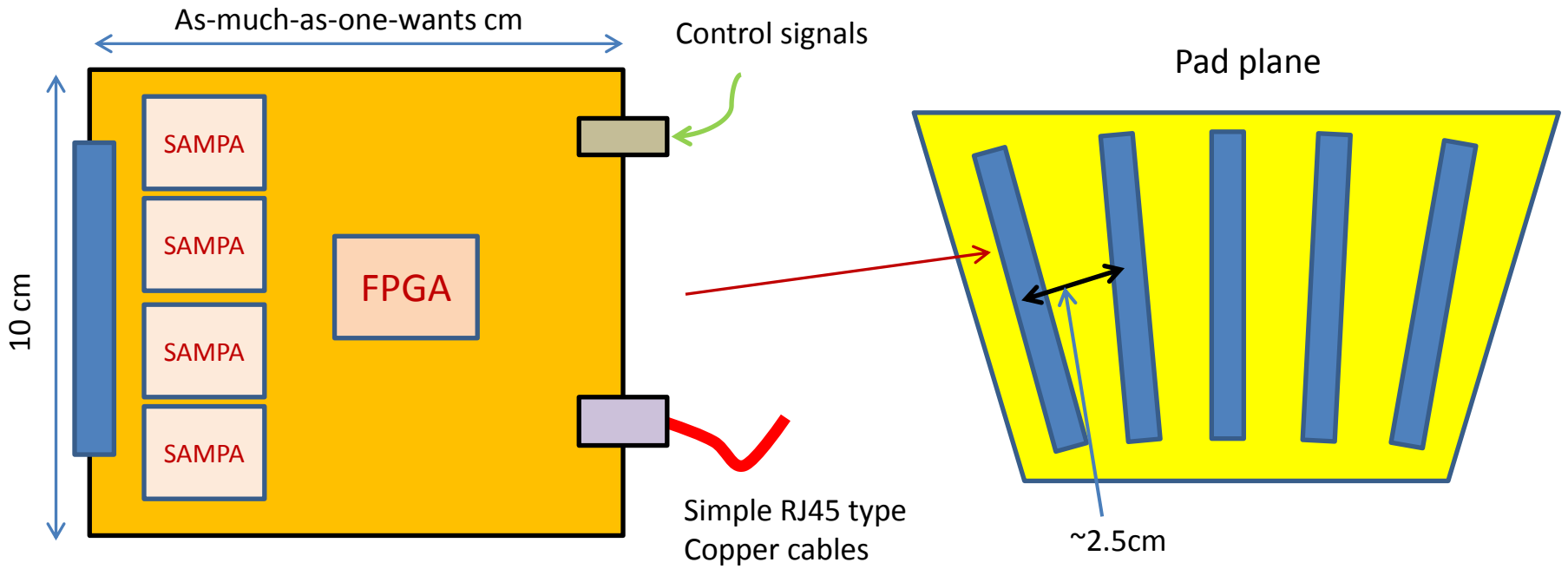


FEE idea

- FEE cards will be directly attached to pad planes
  - 10cm wide for signal input side
  - 4 SAMPAs are placed in parallel. each SAMPA is 15x15mm^2
- FPGA is for handling control and timing signals
- Use one e-link from 1 SAMPA chip.
  - 4 e-link cables from a board
  - Downstream “CRU” takes care of 16 FEE cards

STAR iFEE design





Support Materials

List of questions and initial answers (I)

- Do we trigger events and readout from TPC, or readout continuously? If triggered, the data volume may be reduced
  - TS: may be we should use triggered mode, since continuous mode is not operated in the way we hoped
  - TS: Also, in the trigger mode, the readout fits in PHENIX timing system
- How do we drive the data off from the detector? Copper cable or optical fibers?
  - TS: I think we should use optical fibers. SAMPA has a function to daisy chain data from chip to chip using elink, but Daisy chain among FEE card seems not realistic
- What will be the data format? Does it match to DCM-II?
  - TS: It seems data format from SAMPA is fixed. If we format additionally, we need a FPGA on the FEE board
  - Ed: If we use DCM-II, what function will it do?
- Clusterizers, zero suppression/ADC processing, time stamps
  - TS: zero-suppression and baseline corrections are done in SAMPA. Clustering should be done in the downstream

List of questions and initial answers (II)

- Merging TPC data with other detectors? EvB?
  - TS: If we decide on the trigger mode, TPC data can be merged with the other detectors. In this case, we need EvB.

- Multi-event buffering is possible?
  - TS: SAMPA documentation says that we have to trigger the particular event within 9.6us latency. This may hint that the way that SAMPE buffer the data is similar to the PHENIX readout system, and therefore multi-event buffering is possible

- Do we need an intermediate board (FEM) between FEE and DAQ?
  - TS: I don't think we need except for the receiver of the optical signals. Additional computing should be made

- 15KHZ triggering under 100KHZ beam intensity. What is the maximum tracks would a TPC will see. Is it possible to separate tracks from one event from the others?
  - How about p+p? 40MHz collision rate.
  - TS: It will determine how much samples we should take per event

List of questions and initial answers (III)

- Power consumption of SAMPA
  - TS: 10mW per channel. 320mW/SAMPA. 1.3W for 4 SAMPAs (= one FEE card)
- Packaging of SAMPA
  - TS: the packaging size of SAMPA is 15mm*15mm
  - Chi: SAMPA production schedule?
- Radiation hardness, cooling, cabling, working in magnetic field
  - TS: These items need discussion.
  - Chi: Too strong magnetic field make the commercial DC-DC converter and optical transmitter unworkable
- How much we can copy from STAR and ALICE electronics?
- Show that one can plausibly record 15 kHz of Au+Au with 90% livetime
- Where does the data go? Buffer at 1008, or directly to RCF?
  - Data volume and rate in the other slides

SAMPA chip in detail

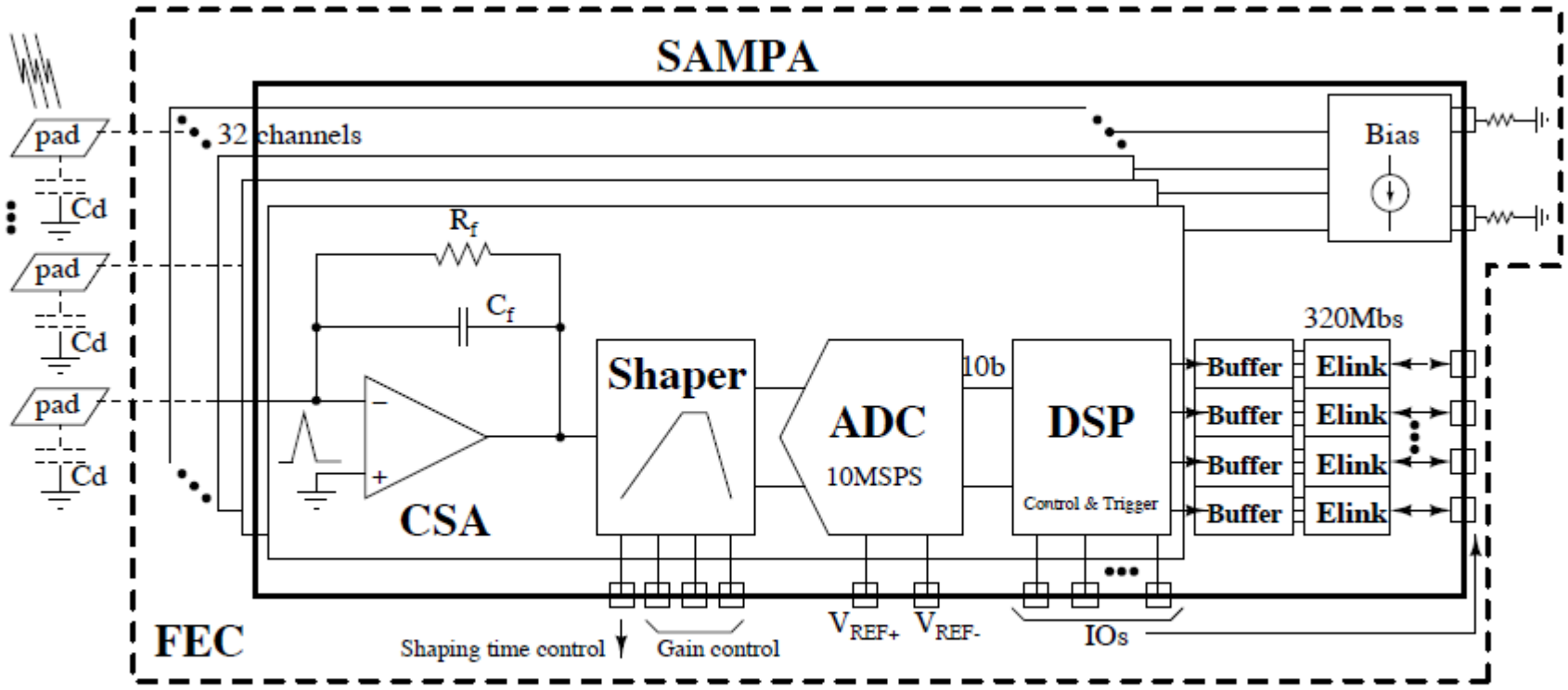
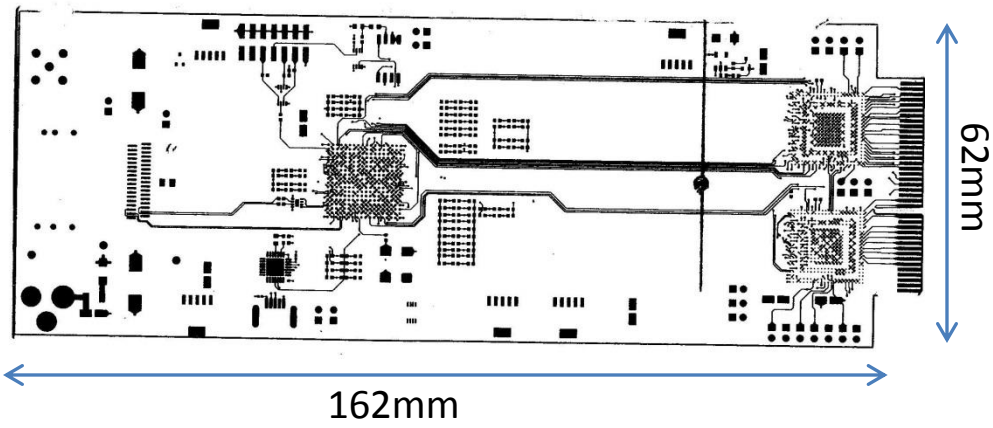
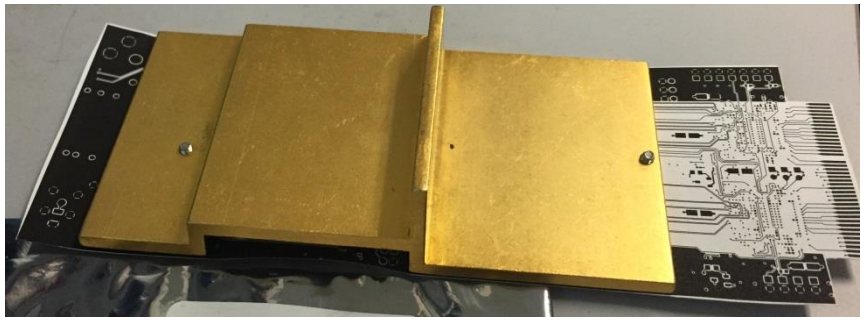


Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

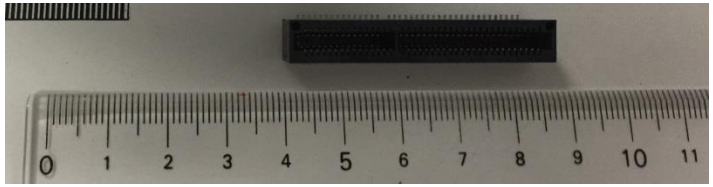
STAR's iFEE

- Good start to think of geometry our front end cards
  - To be attached to pad planes
- Two SAMPA chips on one side of the card
  - Geometry of the card is 62mm*162mm
  - 64 channels/card (32 ch/SAMPA)
  - One SAMPA chip is 15*15mm^2, which is much smaller than I thought
- Input connector is as wide as ~57mm and 10mm in height
  - Takes care of 64 channels. There is one for 160ch also.
- A large heatsink will be attached to the side of the board where no chip is mounted
  - Heatsink is 20mm in height
  - Can be shortened to ~10mm





Input connector (64 channels)



Ref: Readout for ALICE TPC upgrade

- CRU interfaces the FEC and online computer farm
- Through the optical links, both communication, and data transmission are realized

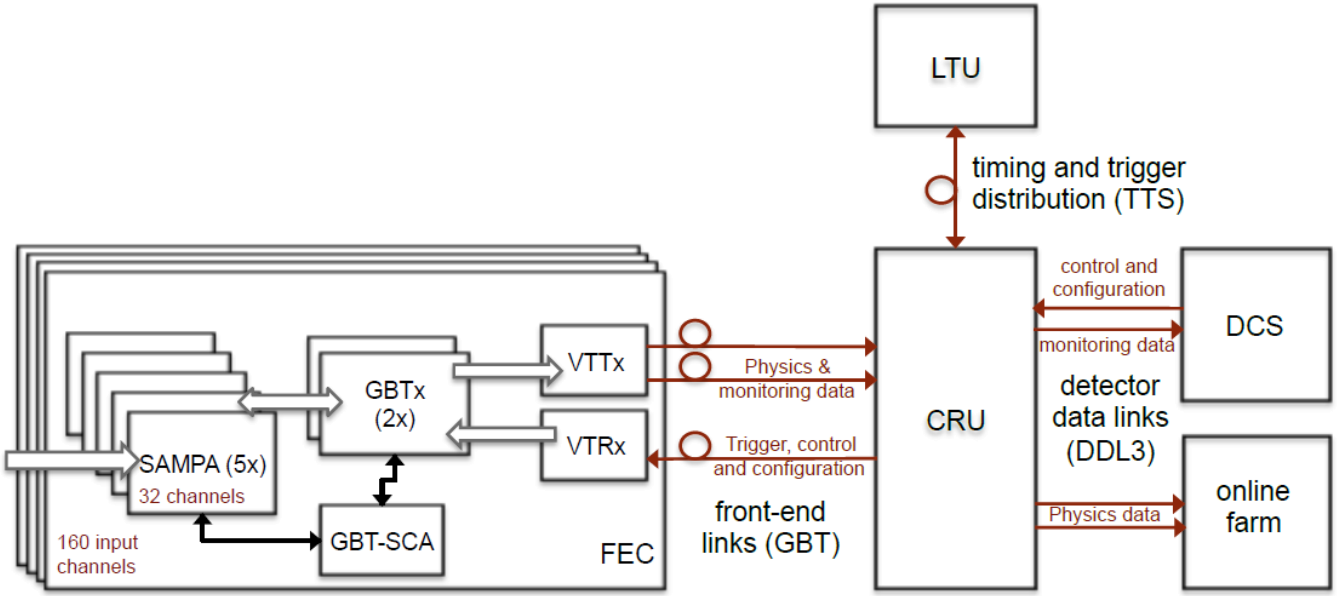
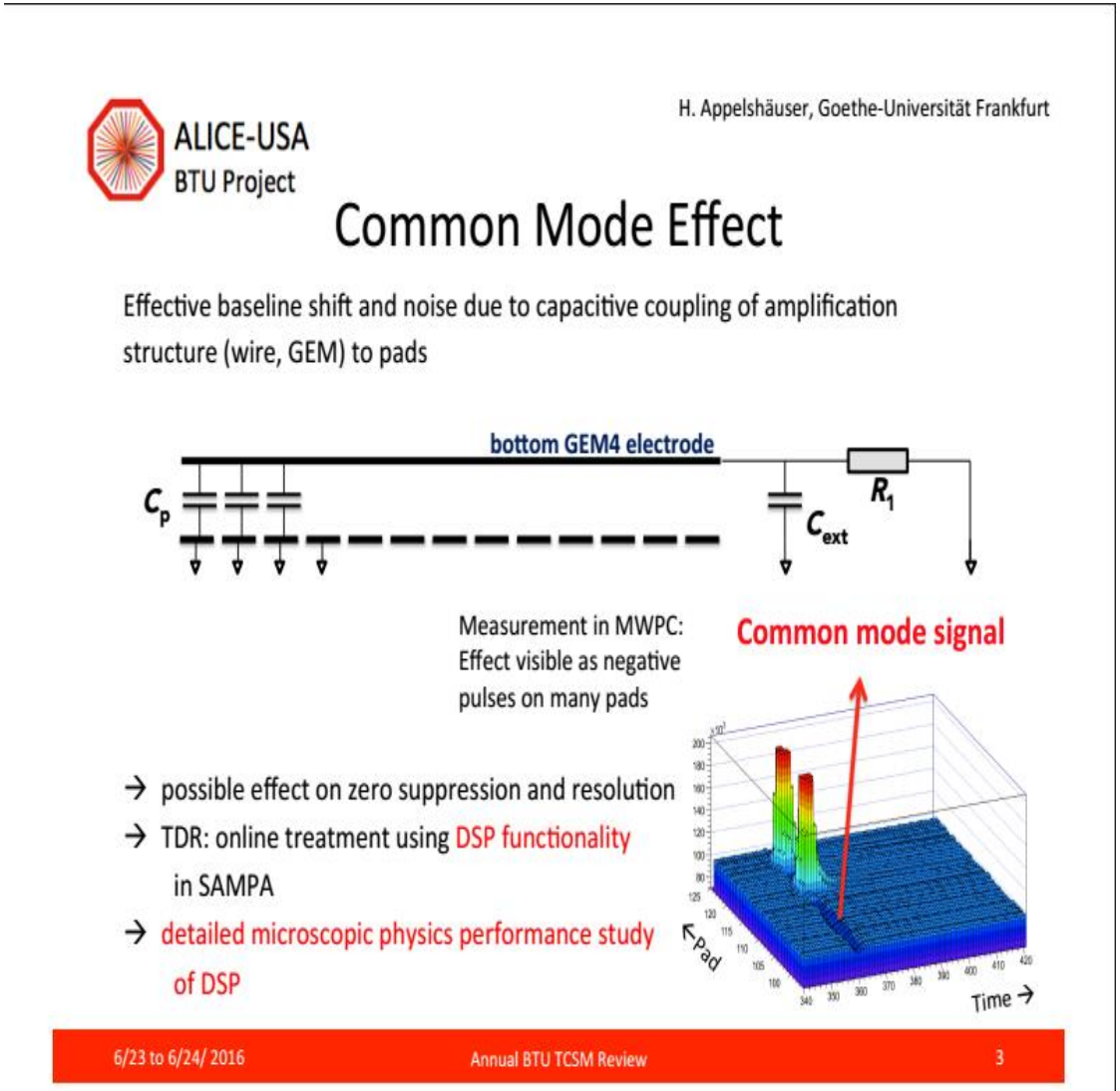


Figure 6.9: Schematic of the TPC readout system with the CRU as central part interfacing the front-end electronics to the trigger system, the DCS and the online farm.

Baseline restoration?

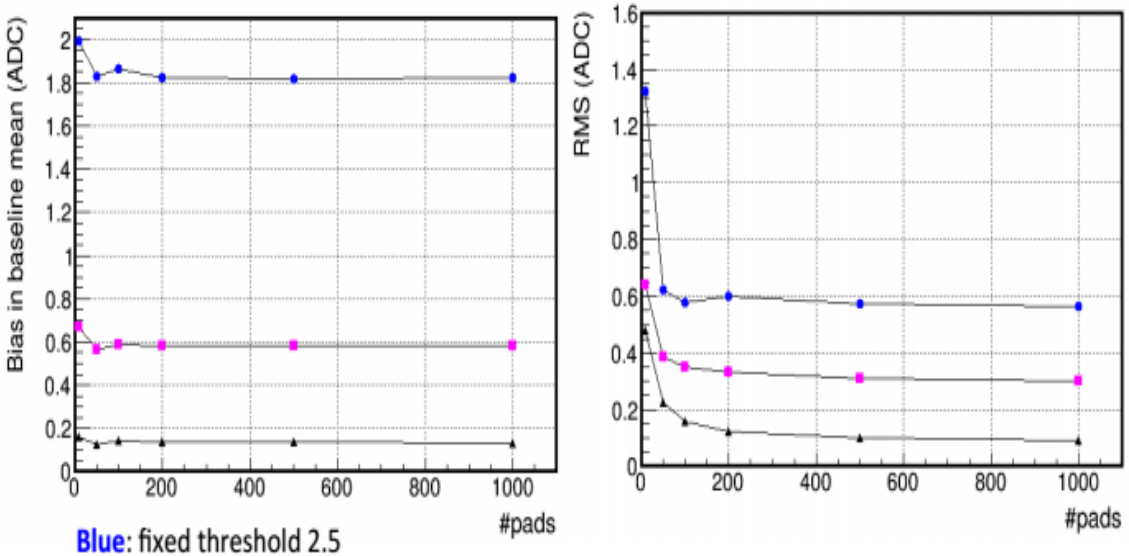


- ALICE's finding of common baseline shift due to capacitive coupling between pads
- Common Mode removal is what the on-board DSP for the SAMPA chip is designed to do.
  - But, this is within a chip, i.e. 32 channels
- The technique:
  - Find a large number of "empty channels".
  - See if they all dip below zero together.
  - Correct everyone up by the amount of the dip.

Their remediation plan and ours

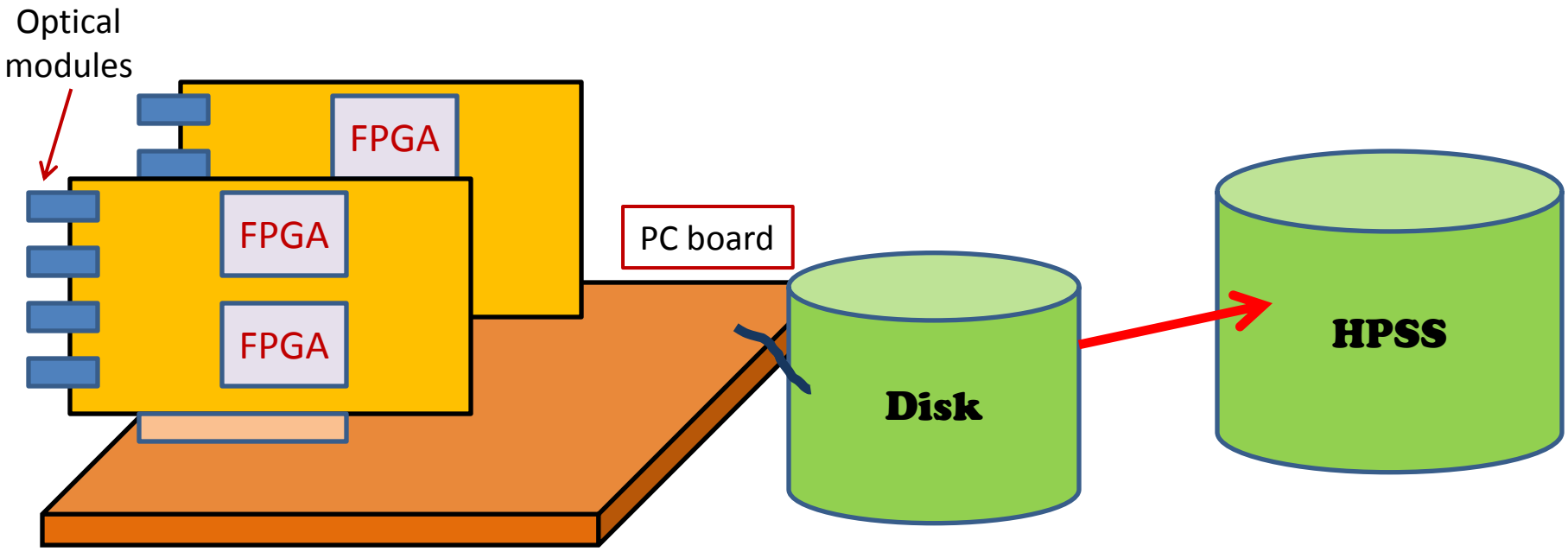
- ALICE's Monte Carlo indicates no improvement in performance beyond 100-200 pads.

- Option for us will be to add a FPGA onto FEE
  - DSP on a SAMPA chip cannot do baseline restoration by importing signals from the other SAMPA chips
  - The FPGA can also be used to format data, (and daisy chaining the data?)



CRM (Continuous Readout Module)

- Assuming 4 channels fiber input
  - Data Volume to be taken care of : 1.6GBytes/card/s or 12Gbits/card/s
- It would be great that the card is realized in a form of PCI Express card?
  - Two cards per DAQ PC?
- Just my idea so far. Needs discussion.
  - BNL instr. division shows strong interest in developing CRM and DAQ part



Costs

- Scaled from the cost estimate for STAR iTPC readout
  - No contingency, labor nor overhead is included

Item	# of items	# with spares (+30%)	$ per item	$ all	ref
SAMPA Chips	6250	8125	$44	$360K	
FEE cards	1563	2032	$150	$305K	
CRM	80	100	$2000	$200K	(arb.)
Cables/fibers				$125K	(STAR *2.5)
Power Supply	120	160	$600	$96K	
DAQ PC	40	50	$8000	$400K	(arb.)
Total				**$1.5M**	

Schedule: based on STAR iTPC case

- Final SAMPA chips are available by the end of 2017
  - Nearly final prototype chip just came out in June
  - We should follow this schedule for FEE card design and production

- CRM part needs another development
  - However, we expect that development/production will be finished by 2021.

Schedule

Presented by Tonko in Jan, 2016

	2016	2017	2018 early	2018 late
padplane	prototype test produce		start sector installation	end sector installation
iFEE	evaluate SAMPA prototype with SAMPA	final version produce 1 sector's worth	produce all PCBs vet PCB purchase all components install into 1 sector & test	SAMPA arrives mount SAMPA & components Q&A install all full system test
iRDO	prototype 2	final version produce 1 sector's worth	produce & Q&A all install into 1 sector & test	install all full system test
Power Supplies Trigger Cables Fibers	evaluate	evaluate test	purchase & install all full test using 1 sector's worth	full system test
Receiver Cards	prototype test	final version	purchase & install all full test using 1 sector's worth	full system test
DAQ PCs	develop drivers	final drivers & software... specification	purchase & install all full test using 1 sector's worth	full system test

Logistics as the summary

- On descoping
  - One option is to read every other radial bin
    - 24 measurements/track. Data volume will be half
  - Material cost will be exactly half

- On collaboration and people power
  - BNL: Ed O'Brien, John Haggerty, Eric Mannel, Martin Purschke, and TS
  - Stony Brook: Tom Hemmick, Chuck Pancake
  - Two STAR people (Bob Sheetz and Tonko Ljubicic) are good advisers
  - Columbia: Cheng-Yi Chi?
  - No engineer involved yet
  - BNL instrumentation division shows strong interest

- On money and near future
  - Currently, we have BNL LDRD money
  - Tonko agreed to provide us two STAR iFEE's (we have to reconfirm), from which we can start evaluating performance as well as readout signals from the prototype TPC